REMARKS

By the present amendment, Claims 1, 4, 5 and 8 have been amended. Claims 1-10 remain pending in the application, with Claims 1, 4-6 and 8 being independent claims. Claims 4 and 5 are rejected under 35 U.S.C. § 101, as allegedly being directed to non-statutory subject matter. Claims 1 and 2 are rejected under35 U.S.C. § 102(e), as allegedly being anticipated by Miyashita (U.S. Patent No. 6,304,611). Claims 4, 5 and 8 are rejected under35 U.S.C. § 102(e), as allegedly being anticipated by Tanaka (U.S. Patent Application Publication No. 2002/0196734 A1). Claims 3, 6 and 7 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Miyashita in view of Tanaka. Claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tanaka in view of Miyashita.

The Examiner states that Claim 4 recites a mathematical algorithm without practical application. The Examiner also states that Claim 5 is deemed non-statutory subject matter based on disclosure in the specification regarding a computer readable medium.

Claims 4 and 5 have been amended to recite, in part, a method of generating an edge sidelobe canceling signal in an orthogonal frequency division multiplexing access system, the method including generating an edge sidelobe canceling signal. These amendments overcome the rejection of Claims 4 and 5 under 35 U.S.C. § 101. Applicants respectfully disagree with comments of the Examiner regarding Claim 5 because Claim 5 recites, in part, a computer program device and not a computer readable medium, as erroneously purported by the Examiner.

The Examiner states that Miyashita teaches all of the recitations of Claims 1 and 2 in col. 2, lines 39-58, col. 5, lines 36-47, col. 7, lines 44-57 and col. 9, lines 33-39. The Examiner states that Tanaka teaches all of the recitations of Claims 4, 5 and 8 in FIGS. 1, 2, and paragraphs 17, 18, 49, 50, 53, 59, 60, 62, 66 and 70.

With respect to Claims 3, 6 and 7, the Examiner concedes that Miyashita does not expressly disclose the uplink communication method. The Examiner states that Tanaka suggests these recitations, and asserts that it would have been obvious to modify Miyashita with the alleged suggestions of Tanaka. With respect to Claims 9 and 10, the Examiner concedes that Tanaka does not expressly disclose recitations regarding wherein when a single subband comprises M subcarriers, the storage unit is implemented by a look-up table. The Examiner states that Miyashita suggests these recitations, and asserts that it would have been obvious to modify Tanaka with the alleged suggestions of Miyashita.

Independent Claim 1 has been amended to recite, in part, an uplink communication method in an orthogonal frequency division multiplexing access system, the method including generating upper and lower edge sidelobe canceling signals in a transmitting terminal for an uplink; and inserting the upper and the lower edge sidelobe canceling signals into guard intervals, respectively, adjacent to a subband allocated to a user and performing inverse fast Fourier transform on user transmission signals and the upper and the lower edge sidelobe canceling signals to be inserted into the guard intervals.

Independent Claim 8 has been amended to recite, in part, apparatus for generating an edge sidelobe canceling signal in an orthogonal frequency division multiplexing access system, the apparatus including a storage unit for storing one of an upper weight vector and a lower weight vector and reading vectors of one of the upper and the lower weight vector in a predetermined order according to an edge sidelobe selection signal; and a matrix operation unit for performing an inner product on a user transmission signal vector and one of the upper and the lower weight vector provided from the storage unit, thereby generating one of an upper and a lower edge sidelobe canceling signal, wherein the apparatus generates an upper edge sidelobe canceling signal corresponding to an inner product of a transmission signal vector of the transmitting terminal and an optimized upper weight vector, and a lower edge sidelobe canceling signal corresponding to an inner product of the transmission signal vector of the

transmitting terminal and an optimized lower weight vector, and allocates the upper and the lower edge sidelobe canceling signals to subcarriers in guard intervals, respectively.

Miyashita describes an OFDM modulator and OFDM modulation method for a digital modulated wave having a guard interval. Miyashita shows, in FIG. 9, an OFDM modulator that includes an IFFT unit 81, a guard interval adder 82, an amplitude controller 1, a symbol edge generator 2, and a quadrature processor 3. Output signals R and I of the IFFT 81 are input to the guard interval adder 82. Signals R_g and I_g obtained by the guard interval adder 82 are input to the amplitude controller 1. The amplitude controller 1 is supplied with a pulse P_E generated at the end edge of the effective symbol duration V_S and a pulse P_S generated at a time point immediately preceding the start of the effective symbol duration. The symbol edge signal generator 2 is supplied with a pulse P_g indicating the guard interval from the guard interval adder 82. The symbol edge signal generator 2 functions to output the pulse P_E representing the end time point of the effective symbol duration and the pulse P_S representing the start time point of the next effective symbol duration to the amplitude controller 1 on the basis of the pulse P_g.

The pulses P_E and P_S output by the symbol edge generator 2 of Miyashita do not correspond to the upper and lower edge sidelobe canceling signals recited in the claims, and Miyashita nowhere provides any teaching or reasonable suggestion to modify the P_E and P_S pulses to arrive at canceling signals in accordance with the present invention.

Tanaka describes an OFDM transmission system transceiver and method. Tanaka shows, in FIG. 1, an OFDM system transceiver that includes a receiver 1, a transmitter 2, antenna elements 10-13 and switches 90-93. During signal transmission, the switches 90-93 disconnect respective S/P converters 20-23 of the receiver 1 from respective antenna elements 10-13, and connect respective multipliers 160-163 of the transmitter 2 to respective antenna elements 10-13. In the transmitter 2, the S/P converter 100 converts serial modulation data into parallel signals. The modulator 110 digitally modulates the parallel signals and

outputs the modulated data to the iFFT 120. The iFFT 120 inverse Fourier-transforms the modulated data into transmission data signals. The P/S converter converts the parallel transmission data signals into serial signals. The weight selector 140 selects a transmission weight by the maximum ratio composition weight W.

Tanaka nowhere suggests generating any of the upper and lower edge sidelobe canceling signals, and Tanaka nowhere provides any teaching or reasonable suggestion to modify the P_E and P_S pulses of Miyashita to arrive at canceling signals in accordance with the present invention. Therefore, Tanaka fails to supplement the deficiencies of Miyashita.

With regard to the Examiner's rejection of claims 1 and 2 under 35 U.S.C. §102(e), Claim 1 has been amended as indicated above. Claims 1 and 2 are not anticipated by Miyashita (U.S.P 6,304,611), in that amended Claim 1 includes processes performed in the front stage of an inverse fast Fourier transformer (IFFT) while Miyashita includes only a series-parallel conversion process in the front stage of IFFT. In addition, amended Claim 1 includes inserting upper and the lower edge sidelobe canceling signals into guard intervals, respectively, adjacent to a subband allocated to a user and performing inverse fast Fourier transformation on user transmission signals and the upper and the lower edge sidelobe canceling signals to be inserted into the guard intervals.

With regard to the Examiner's rejection of Claims 3, 6 and 7 under 35 U.S.C. §103(a), Claims 3, 6 and 7 are patentable over Miyashita in view of Tanaka, in that each of Claims 3, 6 and 7 includes processes performed in the front stage of IFFT while both Miyashita and Tanaka include only a series-parallel conversion process in the front stage of IFFT. In particular, neither Miyashita nor Tanaka discloses obtaining the upper and the lower edge sidelobe canceling signals by performing an inner product on a transmission signal vector of the transmitting terminal and an optimized upper weight vector and performing an inner product on the transmission signal vector of the user transmitting terminal and an optimized lower weight vector, respectively, which is included in each of Claims 3, 6 and 7. In addition, in Miyashita,

Ps pulses are generated in synchronization with a falling edge and a rising edge of a signal Pg indicating a guard interval, and the amplitude of a complex carrier signal provided from a guard interval adder 82 after an IFFT unit 81 is attenuated at a respective period of Ps pulse Ps pulse, while Claims 3, 6 and 7 include performing inverse fast Fourier transformation on user transmission signals and the upper and the lower edge sidelobe canceling signals to be inserted into the guard intervals.

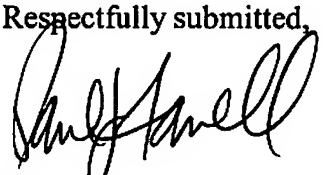
More particularly, Miyashita, Tanaka, or any combination thereof, fails to teach or reasonably suggest an uplink communication method in an orthogonal frequency division multiplexing access system, the method including generating upper and lower edge sidelobe canceling signals in a transmitting terminal for an uplink; and inserting the upper and the lower edge sidelobe canceling signals into guard intervals, respectively, adjacent to a subband allocated to a user and performing inverse fast Fourier transform on user transmission signals and the upper and the lower edge sidelobe canceling signals to be inserted into the guard intervals, as recited in Claim 1. Miyashita, Tanaka, or any combination thereof, also fails to teach or reasonably suggest similar recitations in Claims 4-6 and 8.

Accordingly, amended Claims 1, 4-6 and 8 are allowable over Miyashita, Tanaka, or any combination thereof.

While not conceding the patentability of the dependent claims, *per se*, Claims 2, 3 and 5-10 are also allowable for at least the above reasons.

Accordingly, all of the claims pending in the Application, namely, Claims 1-10, are in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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